What is claimed is:

1. A circuit board having two sides, the circuit board comprising:

a substrate having a first array of vias to connect to a first agent, the first array of vias defining a first set of channels on the substrate, and having a second array of vias to connect to a second agent, the second array of vias defining a second set of channels on the substrate; and

a bus comprising bus traces, wherein each bus trace is routed in only one channel belonging to the first set of channels and routed in only one channel belonging to the second set of channels.

2. The circuit board as set forth in claim 1, wherein the first and second agents are mounted upon only one of the two sides of the circuit board.

3. The circuit board as set forth in claim 1, wherein the bus propagates a source synchronous clock signal having a source synchronous clock frequency and a common clock signal having a common clock frequency,

wherein the source synchronous clock frequency is at least twice the common clock frequency.

4. The circuit board as set forth in claim 3, wherein the first and second agents are mounted upon only one of the two sides of the circuit board.

5. The circuit board as set forth in claim 1, wherein the first array of vias are arranged in substantially linear rows and the second array of vias are arranged in substantially linear rows.

6. An electronic system comprising:

a circuit board having a first trace segment and a second trace segment; and

an interconnector supported by the circuit board, the interconnector having a third trace segment connected to the first trace segment by way of a first via, and having a fourth trace segment connected to the second trace segment by way of a second via.

7. The electronic system as set forth in claim 6, wherein first, second, third, and fourth trace segments have substantially equivalent characteristic impedances.

8. The electronic system as set forth in claim 6, further comprising:

a die; and

a die package to support the die, the die package having a stub connected to the third and fourth trace segments by way of a third via, wherein the first, second, third, and fourth trace segments form a bus trace.

9. A circuit board comprising:

a conductive plane having de-gassing holes;

a first bus trace substantially parallel to the conductive plane;

a second bus trace substantially parallel to the conductive plane; and

a dielectric disposed between the conductive plane and the first and second bus traces, the combination of the first and second bus traces with the conductive plane and dielectric having, respectively, first and second characteristic impedances and to guide electromagnetic radiation having a wavelength, wherein the de-gassing holes are substantially smaller than the wavelength, and wherein the first and second bus traces are positioned relative to the de-gassing holes so that the first and second characteristic impedances are substantially equal to each other.

10. The circuit board as set forth in claim 9, wherein the de-gassing holes have diameters less than one-tenth of the wavelength.

11. A circuit board comprising:

a conductive plane having de-gassing holes;

a first bus trace substantially parallel to the conductive plane;

a second bus trace substantially parallel to the conductive plane; and

a dielectric disposed between the conductive plane and the first and second bus traces, the combination of the first and second bus traces with the conductive plane and dielectric to guide electromagnetic radiation having a wavelength, wherein the de-gassing holes are substantially smaller than the wavelength, wherein the first bus trace passes over a first local average of de-gassing holes per unit length, wherein the second bus trace passes over a second local average of de-gassing holes per unit length, and wherein the first and second bus traces are positioned relative to the de-gassing holes so that the first

and second local averages of de-gassing holes per unit length are substantially equal to each other.

12. The circuit board as set forth in claim 11, wherein the second and first local averages are taken over one quarter of the wavelength.

13. The circuit board as set forth in claim 11, wherein the de-gassing holes have diameters less than one-tenth of the wavelength.

14. A circuit board comprising:

a substrate having an array of vias, the array of vias defining a set of channels on the substrate; and

three bus traces routed on the circuit board so as to enter a first channel belonging to the set of channels and to exit a second channel belonging to the set of channels, the first and second channels adjacent to each other so that there is one row of vias between the first and second channels, wherein each of the three bus traces are connected to a via belonging to the row of vias so as to define three connections, wherein the three connections do not overlap the three bus traces.